	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	1028	(712/235,237-240).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:06
2	BRS	L2	96	1 and branch adj control	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:07
3	BRS	L3	70	2 and target adj address and 'branch target address cache'	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:10
4	BRS	L4	20972613	@ad<"20010703"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:09
5	BRS	L5	55	3 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:09
6	BRS	L6	15	5 and (selection adj logic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:10

7	BRS	L7	10	6 and instruction adj buffer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:10

	Type	L #	Hits	Search Text	DBs	Time Stamp
8	BRS	L8	104	(target adj address and 'branch target address cache' and 'instruction buffer').clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:11
9	BRS	L9	104	('instruction cache' and target adj address and 'branch target address cache' and 'instruction buffer').clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:12
10	BRS	L10	55	('branch control' and 'instruction cache' and target adj address and 'branch target address cache' and 'instruction buffer').clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:12
11	BRS	L11	45	('branch control' same 'instruction cache' and target adj address and 'branch target address cache' and 'instruction buffer').clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:12
12	BRS	L12	31	('branch control' same 'instruction cache' same target adj address and 'branch target address cache' and 'instruction buffer').clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:12
13	BRS	L13	30	('branch control' same 'instruction cache' same target adj address same 'branch target address cache' and 'instruction buffer').clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:13

14	BRS	L14	30	('branch control' same 'instruction cache' same target adj address same 'branch target address cache' same 'instruction buffer').clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2006/04/02 15:13

	Type	L #	Hits	Search Text	DBs	Time Stamp
15	BRS	L15	16	('branch control' same 'instruction cache' same target adj address same 'branch target address cache' same 'instruction buffer').clm.	US-PGPUB	2006/04/02 15:14
16	BRS	L16	16	('branch instruction' same 'branch control' same 'instruction cache' same target adj address same 'branch target address cache' same 'instruction buffer').clm.	US-PGPUB	2006/04/02 15:16
17	BRS	L17	8	('fetched address' same 'branch instruction' same 'branch control' same 'instruction cache' same target adj address same 'branch target address cache' same 'instruction buffer').clm.	US-PGPUB	2006/04/02 15:17
18	BRS	L18	2	('multiplexer' same 'fetched address' same 'branch instruction' same 'branch control' same 'instruction cache' same target adj address same 'branch target address cache' same 'instruction buffer').clm.	US-PGPUB	2006/04/02 15:17